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IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re patent application of

Amy J. Gottsche, et al.

Docket No.: BUR920030165US1

Serial No.: 10/710802

Group Art Unit: Unassigned

Filed: 08/04/04

Examiner: Unassigned

For: **SEGMENTED ALGORITHMIC PATTERN GENERATOR**

Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450

SUPPLEMENTAL INFORMATION DISCLOSURE STATEMENT

Sir:

Under the provisions of 37 CFR §1.97 through §1.99 and pursuant to applicant's duty of disclosure under 37 CFR §1.56, applicant respectfully brings the following documents, listed on the attached form PTO-1449, to the attention of the Examiner in charge of the above-identified application. A copy of the cited references is enclosed for the convenience of the Examiner.

This citation does not constitute an admission that the references are relevant or material to the claims. They are only cited as constituting related art of which the applicant is aware.

It is respectfully requested that the listed references be considered by the Examiner and formally made of record in this application.

Please charge any deficiencies in fees and credit any overpayment of fees to International Business Machines Corporation's deposit account no. 09-0456.

Respectfully submitted,

Andrew M. Calderon
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Supplemental Form PTO-1449 (Modified)	Attorney Docket No.: BUR920030165US1	Serial No: 10/710802
LIST OF PATENTS AND PUBLICATIONS FOR APPLICANT'S INFORMATION DISCLOSURE STATEMENT	Applicant: Amy J. Gottsche, et al.	
(Use several sheets if necessary) Page 1 of 1	Filing Date: 08/04/04	Group: Unassigned

REFERENCE DESIGNATION

U.S. PATENT DOCUMENTS

EXAMINERS INITIALS		DOCUMENT NUMBER	DATE	NAME	CLASS	SUBCLASS	FILING DATE (IF APPRO.)

FOREIGN PATENT DOCUMENTS

		DOCUMENT NUMBER	DATE	COUNTRY	CLASS	SUBCLASS	TRANSLATION YES	TRANSLATION NO
		2-24584	01-26-1990	Japan			☒ Abstract	☐
		2001-349930	12-21-2001	Japan			☒ Abstract	☐
							☐	☐
							☐	☐
							☐	☐

OTHER ART (Including Author, Title, Date, Pertinent Pages, etc.)

			C.W. Cha, et al., "Array Test Pattern Generation Algorithms for a Per Pin Tester", IBM Technical Disclosure Bulletin, Vol. 30, No. 10, March 1988.
			J.T. Muhr, et al., "Test Pattern Generation for Partitioned Programmable Logic Arrays", IBM Technical Disclosure Bulletin, Vol. 26, No. 3B, August 1983.
			P.Y.W. Au, et al., "Technique for VLSI In-Circuit Testing", IBM Technical Disclosure Bulletin, Vol. 31, No. 4, September 1988.

EXAMINER	DATE CONSIDERED

EXAMINER: Initial if reference considered, whether or not citation is in conformance with MPEP 609. Draw line through citation if not conformance and not considered. Include copy of this form with next communication to applicant.